

Figure 1

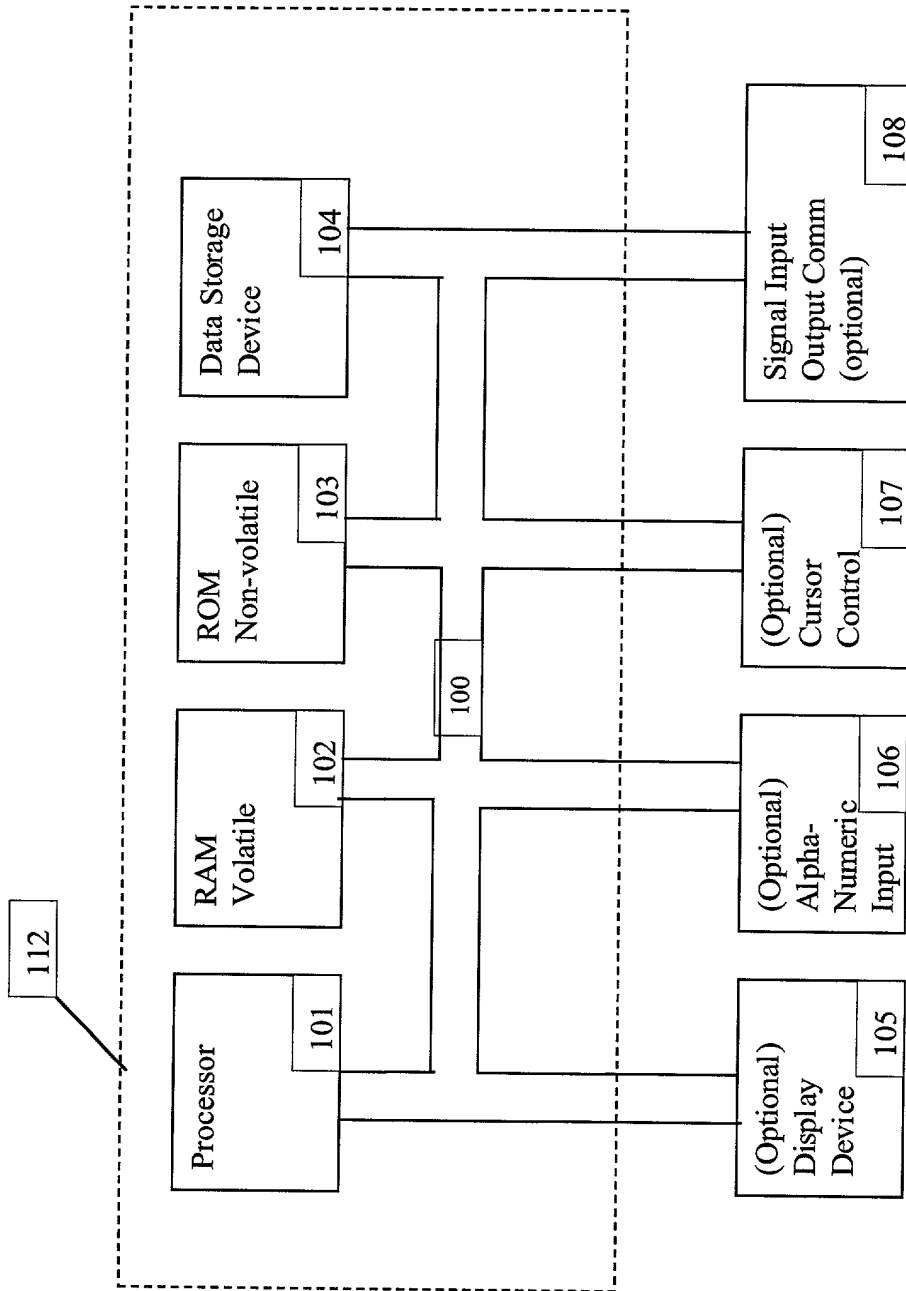


Figure 2

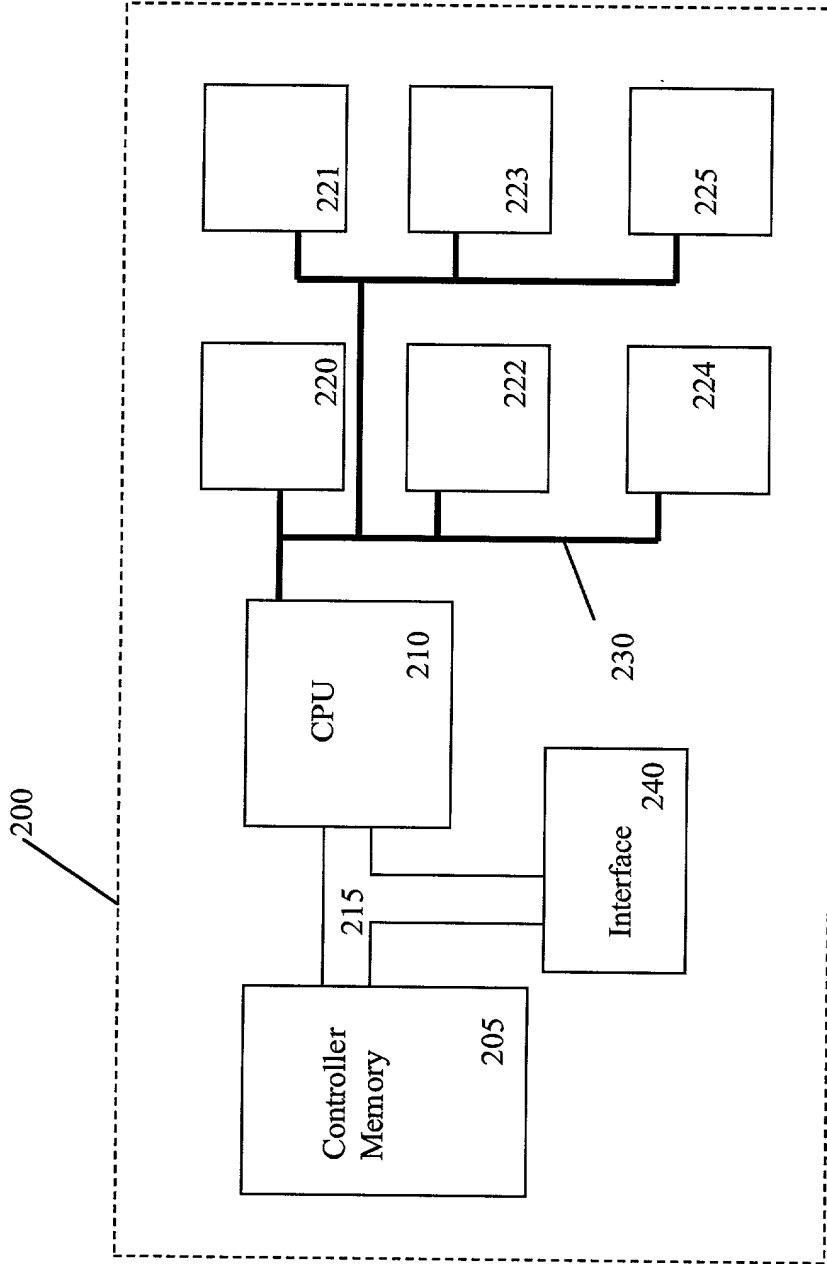


Figure 3

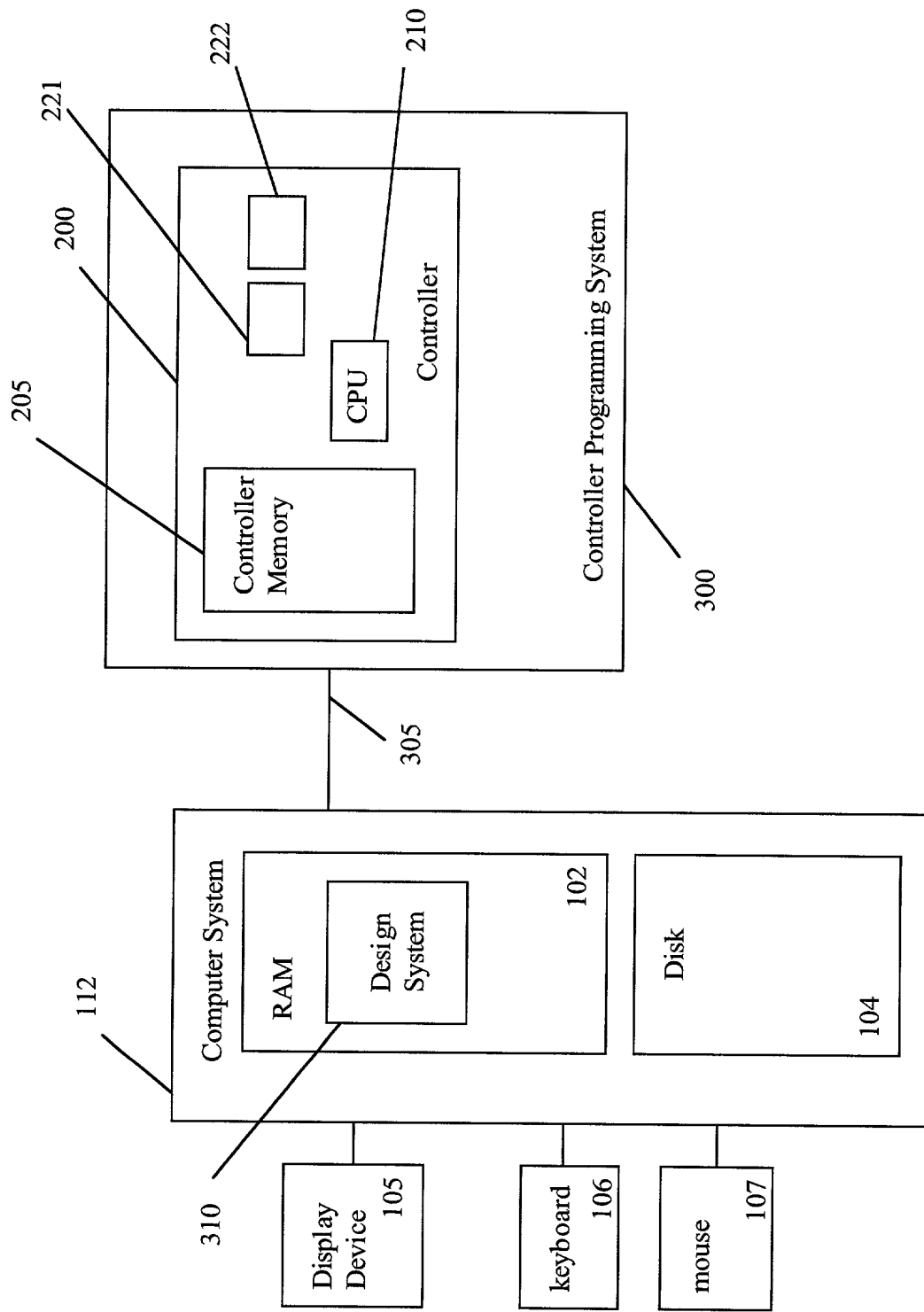
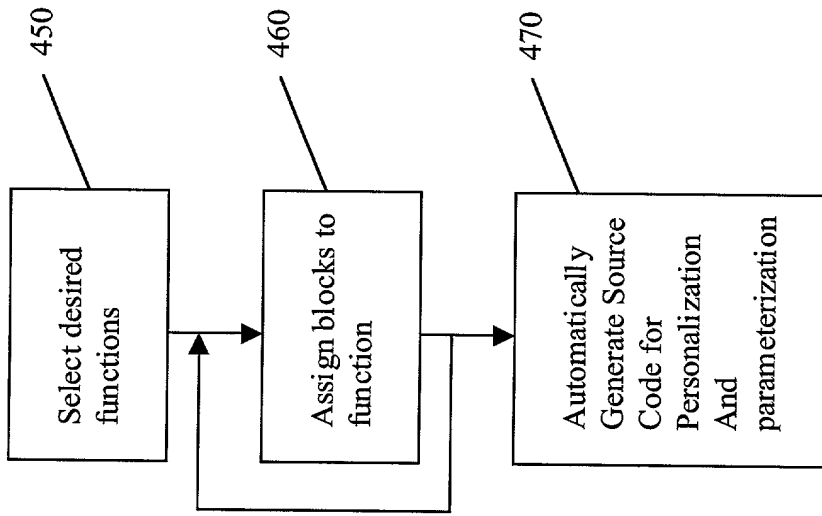
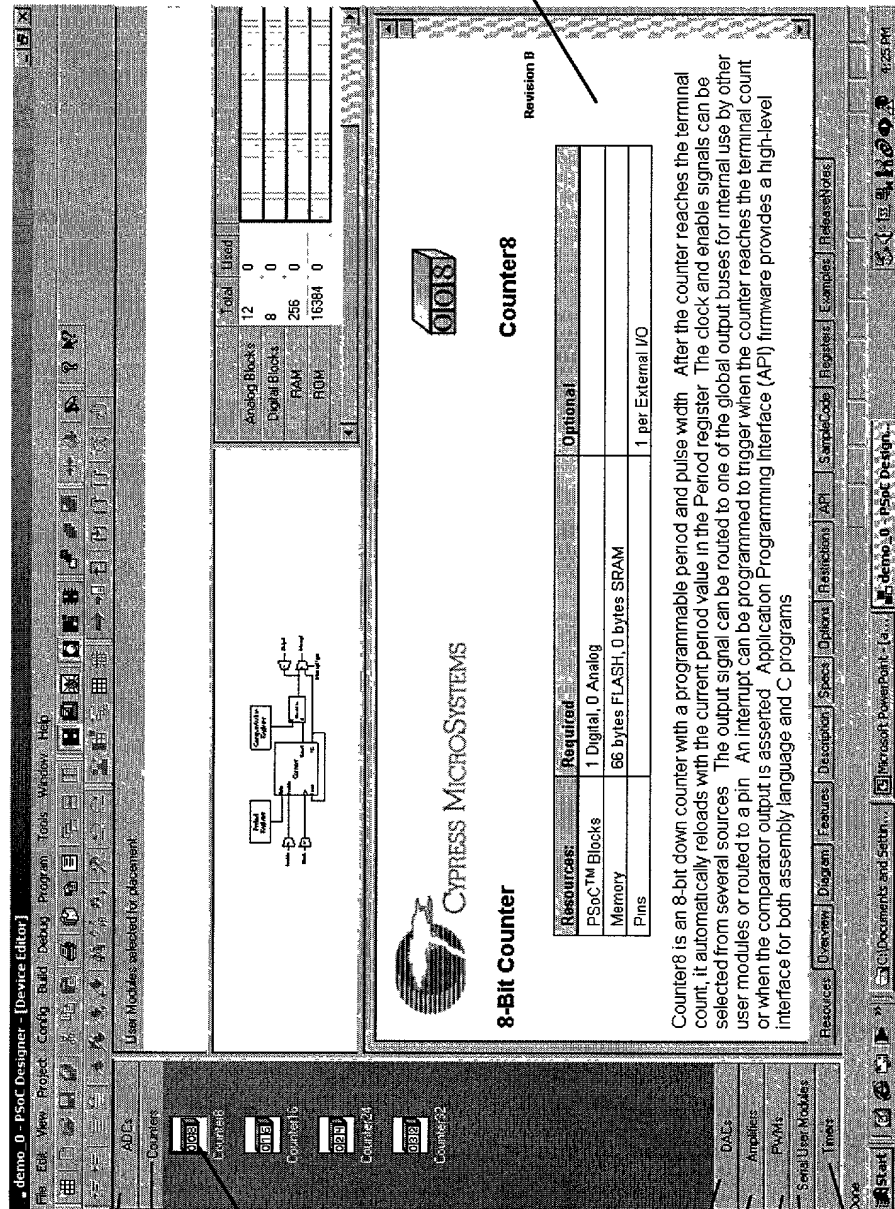


Figure 4



[illegible]

1. *Chlorophyll a* (Chl *a*)  
 2. *Chlorophyll b* (Chl *b*)  
 3. *Chlorophyll c* (Chl *c*)  
 4. *Chlorophyll d* (Chl *d*)  
 5. *Chlorophyll e* (Chl *e*)  
 6. *Chlorophyll f* (Chl *f*)  
 7. *Chlorophyll g* (Chl *g*)  
 8. *Chlorophyll h* (Chl *h*)  
 9. *Chlorophyll i* (Chl *i*)  
 10. *Chlorophyll j* (Chl *j*)  
 11. *Chlorophyll k* (Chl *k*)  
 12. *Chlorophyll l* (Chl *l*)  
 13. *Chlorophyll m* (Chl *m*)  
 14. *Chlorophyll n* (Chl *n*)  
 15. *Chlorophyll o* (Chl *o*)  
 16. *Chlorophyll p* (Chl *p*)  
 17. *Chlorophyll q* (Chl *q*)  
 18. *Chlorophyll r* (Chl *r*)  
 19. *Chlorophyll s* (Chl *s*)  
 20. *Chlorophyll t* (Chl *t*)  
 21. *Chlorophyll u* (Chl *u*)  
 22. *Chlorophyll v* (Chl *v*)  
 23. *Chlorophyll w* (Chl *w*)  
 24. *Chlorophyll x* (Chl *x*)  
 25. *Chlorophyll y* (Chl *y*)  
 26. *Chlorophyll z* (Chl *z*)  
 27. *Chlorophyll aa* (Chl *aa*)  
 28. *Chlorophyll ab* (Chl *ab*)  
 29. *Chlorophyll ac* (Chl *ac*)  
 30. *Chlorophyll ad* (Chl *ad*)  
 31. *Chlorophyll ae* (Chl *ae*)  
 32. *Chlorophyll af* (Chl *af*)  
 33. *Chlorophyll ag* (Chl *ag*)  
 34. *Chlorophyll ah* (Chl *ah*)  
 35. *Chlorophyll ai* (Chl *ai*)  
 36. *Chlorophyll aj* (Chl *aj*)  
 37. *Chlorophyll ak* (Chl *ak*)  
 38. *Chlorophyll al* (Chl *al*)  
 39. *Chlorophyll am* (Chl *am*)  
 40. *Chlorophyll an* (Chl *an*)  
 41. *Chlorophyll ao* (Chl *ao*)  
 42. *Chlorophyll ap* (Chl *ap*)  
 43. *Chlorophyll aq* (Chl *aq*)  
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Figure 8A

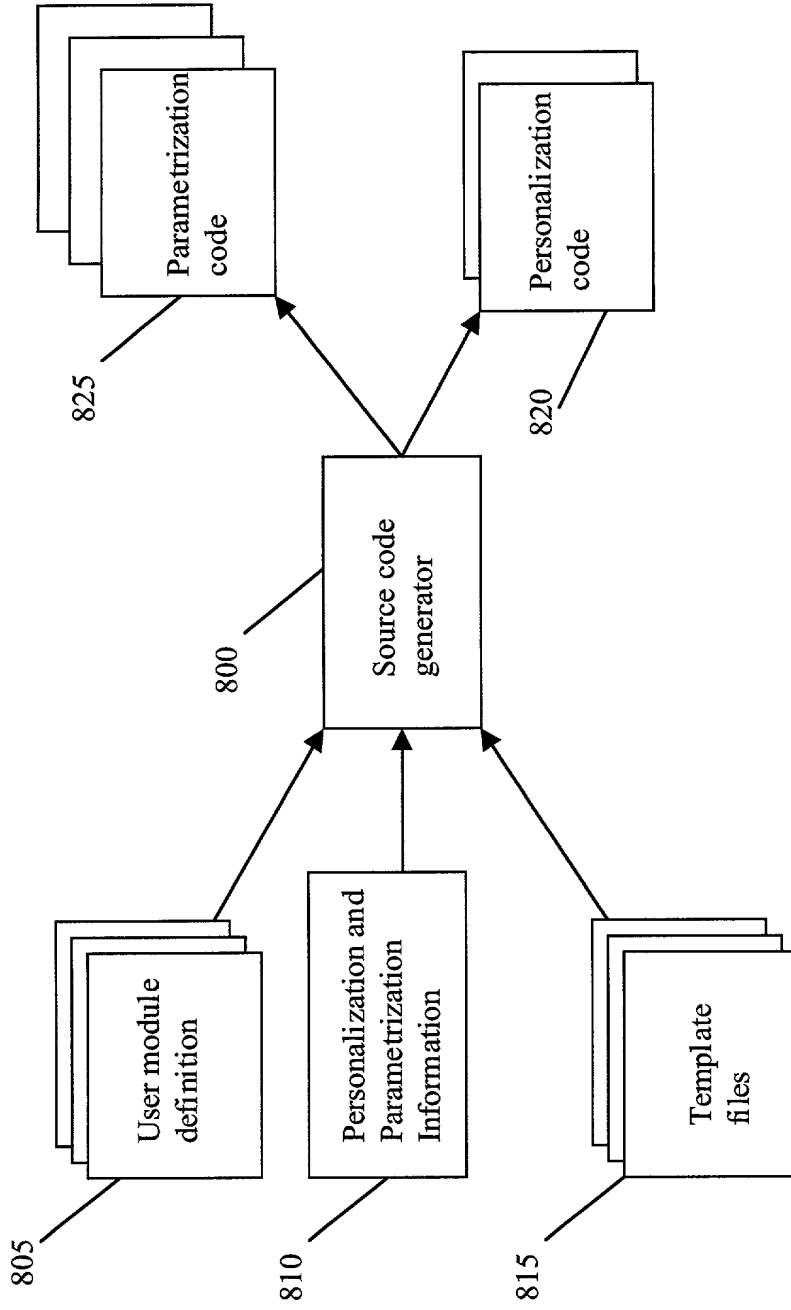




Figure 8B

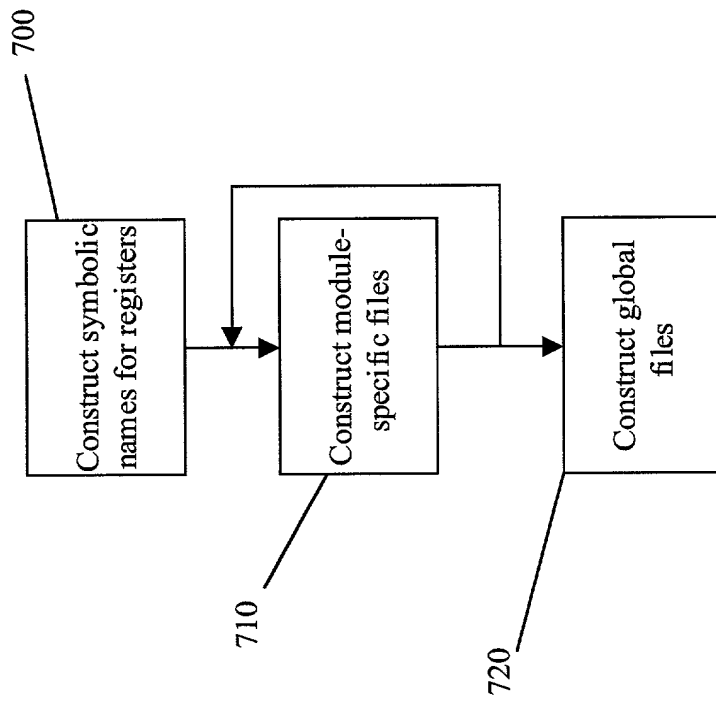


Figure 9

```

;-----
; Interrupt Vector Table
;-----
; Interrupt vector table entries are 4 bytes long and contain the code
; that services the interrupt (or causes it to be serviced).
;-----

AREA TOP(ROM, ABS)

org 0          ; Reset Interrupt Vector
jmp __start    ; First instruction executed following a Reset

org 04h        ; Supply Monitor Interrupt Vector
'@INTERRUPT_1'
ret

633
org 08h        ; PSoc Block DBA00 Interrupt Vector
'@INTERRUPT_2'
ret
```

Figure 10

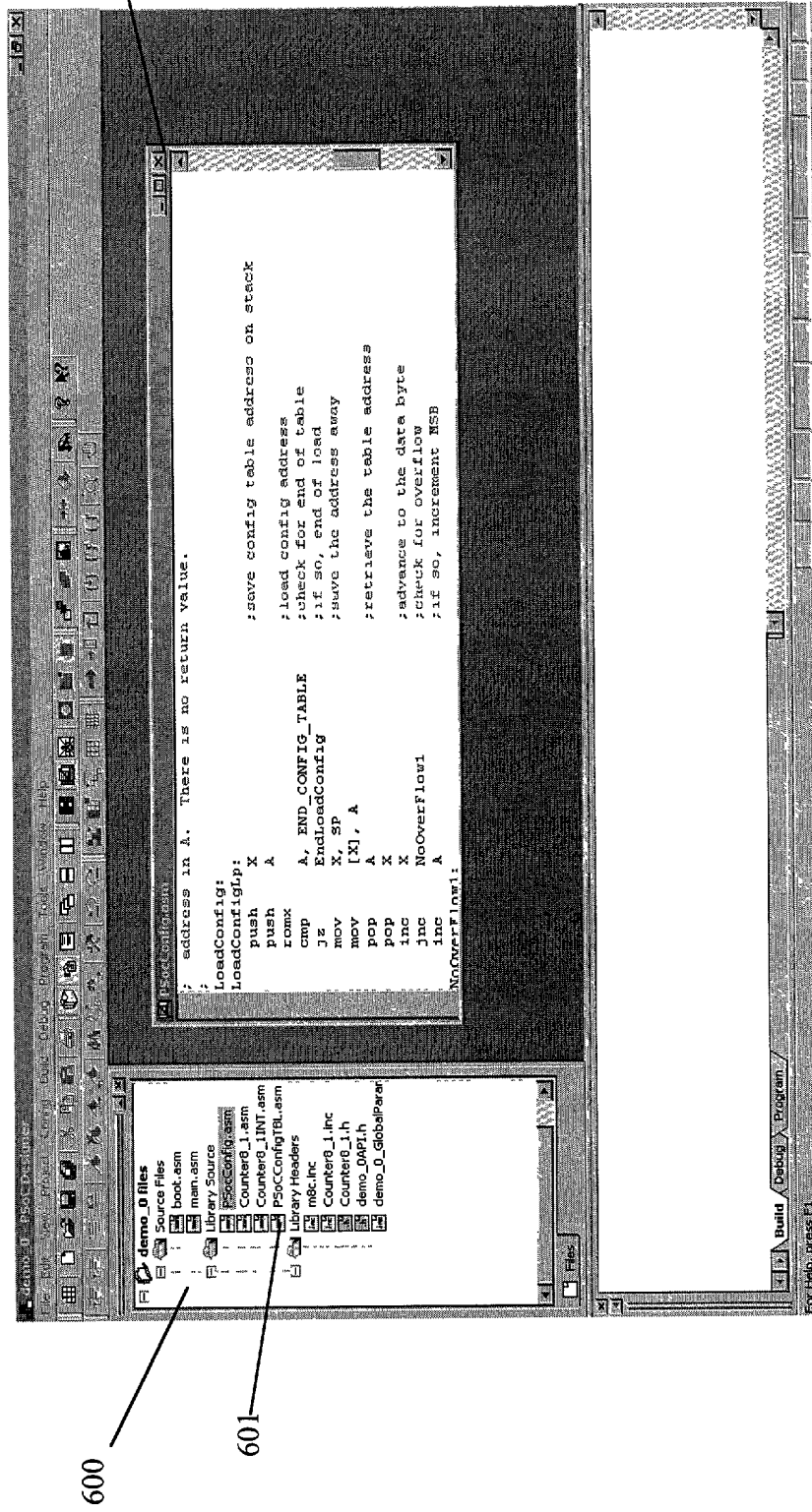


Figure 11

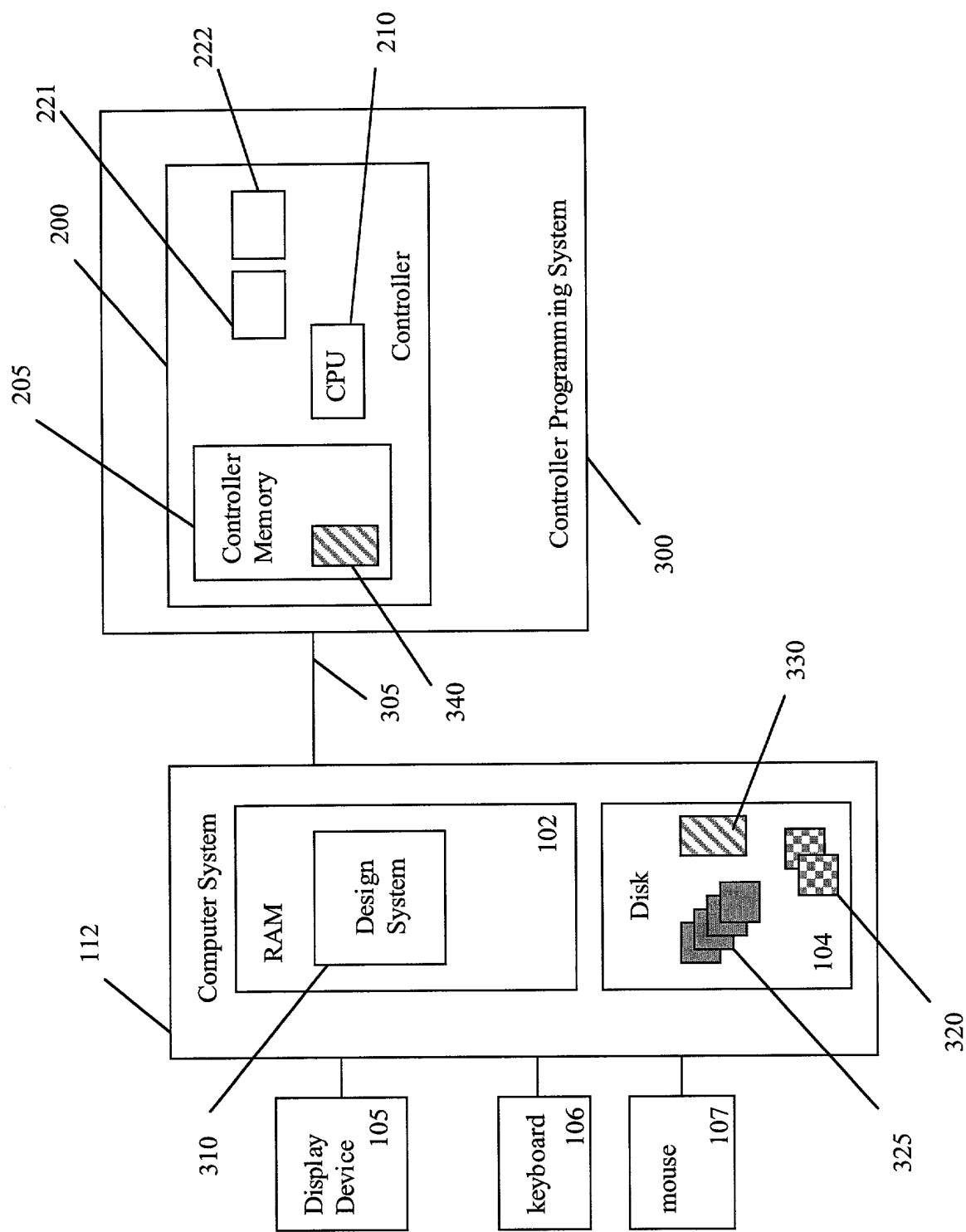


Figure 12

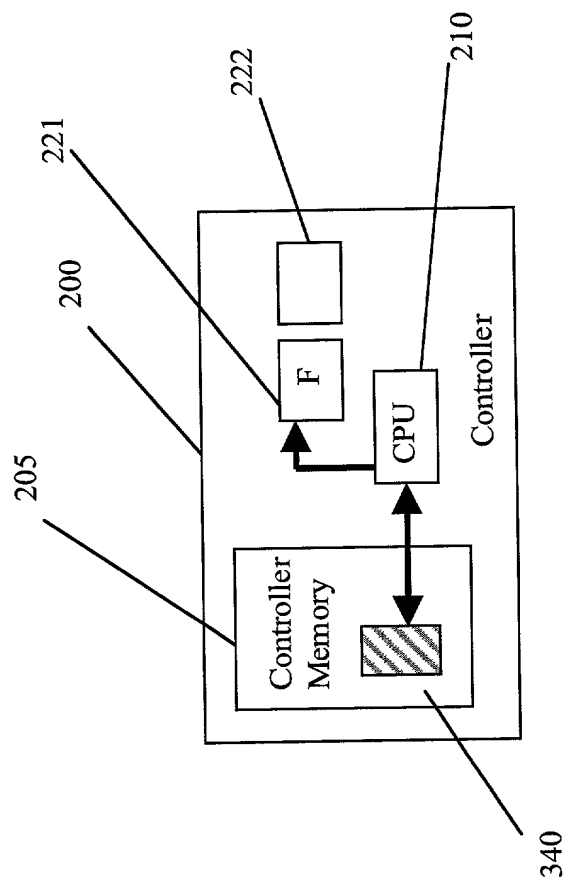


Figure 13

```

LoadConfigTBL_demo_0_Bank0:
; Global Register values
db 60h, 28h
db 63h, 05h
db 65h, 00h
db e6h, 00h
db 02h, 03h
db 06h, 00h
db 0ah, 00h
db 0eh, 00h
db 12h, 00h
db 16h, 00h

; Instance name Counter8_1, User Module Counter8
; Instance name Counter8_1, Block Name CNTR8(DBA02)
db 2bh, 00h
db 29h, 0ch
db 2ah, 04h
db fffh

; AnalogColumnInputSelect register
; AnalogReferenceControl register
; AnalogSyncControl register
; DecimatorControl register
; Port_0_Bypass register
; Port_1_Bypass register
; Port_2_Bypass register
; Port_3_Bypass register
; Port_4_Bypass register
; Port_5_Bypass register

; Counter8_1_CONTROL_REG
; Counter8_1_PERIOD_REG
; Counter8_1_COMPARE_REG

```

Figure 14

```
;
; THEORY of OPERATION:
;   Write data into the Period register.
;
;-----
Counter8_1_WritePeriod:
Counter8_1_WritePeriod:
mov REG[Counter8_1_PERIOD_REG ],A
ret
```

Figure 15

```

;-----
; Registers used by counter8
;-----
Counter8_1_CONTROL_REG: equ 2bh ;Control register
Counter8_1_COUNTER_REG: equ 28h ;Counter register
Counter8_1_PERIOD_REG : equ 29h ;Period value register
Counter8_1_COMPARE_REG: equ 2ah ;Compare Value register
Counter8_1_FUNC_REG : equ 28h ;Function register
Counter8_1_INPUT_REG : equ 29h ;Input register
Counter8_1_OUTPUT_REG : equ 2ah ;Output register

; end of file

```



Figure 16

```

/*****
* Prototypes of Counter8 API. For a definition of
* functions see Counter8_1.inc.
*****/

extern void Counter8_1_EnableInt(void);
extern void Counter8_1_DisableInt(void);
extern void Counter8_1_Start(void);
extern void Counter8_1_Stop(void);
extern void Counter8_1_WritePeriod(BYTE bPeriod);
extern void Counter8_1_WriteCompareValue(BYTE bCompareValue);
extern BYTE bCounter8_1_ReadCompareValue(void);
extern BYTE bCounter8_1_ReadCounter(void);

```